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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,362	07/15/2003	Chien-Hui Chuang	FTCP0022USA	1361
27765	7590	07/12/2005	EXAMINER	
NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)			PATEL, DHARTI HARIDAS	
P.O. BOX 506			ART UNIT	
MERRIFIELD, VA 22116			PAPER NUMBER	

2835

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/604,362

Applicant(s)

CHUANG ET AL.

Examiner

Dharti H. Patel

Art Unit

2835

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 9 is/are rejected.
- 7) ☒ Claim(s) 6-8, 10 and 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07/15/2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Detailed Action

1. ***Claim Rejections - 35 USC § 112***

Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 9 is unclear in that it refers to a third PMOS transistor, however fails to disclose a second PMOS transistor. Correction and/or clarification is required.

2. ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al, Patent No. 6,690,561, in view of Carobolante, Patent No. 5,550,497. Hung et al. teaches an ESD protection circuit that utilizes the resistor-capacitor (RC) branch 1700, Fig 10 as a voltage generator electrically connected to a first node N1 for generating a voltage as disclosed in Col. 6, lines 4-6, and lines 10-11. Hung et al. further teaches a first PMOS transistor 608 having a source electrically connected to the voltage source, a gate electrically connected to the first node N1, and a drain electrically connected to a second node N2; a first NMOS transistor 610 having a drain electrically connected to the second node N2, a gate electrically connected to the first node

N1, and a source connected to ground; a second NMOS transistor 616 having a drain electrically connected to the voltage source, a gate electrically connected to the second node N2, and a source connected to ground as explained in Col. 6, lines 12-25, 29-32 and Fig. 6A. However, Hung et al. does not disclose a second PMOS transistor having a source electrically connected to the second node, a gate and a drain both electrically connected to the first node.

Carobolante teaches a similar technique in his invention of power driver circuit that utilizes a design of a zener diode 34, for preventing an over-voltage condition, which is connected between the first node N1 and the second node N2 as disclosed in Col. 5, lines 30-34 and Fig. 3. Therefore it would have been obvious to one of ordinary skill in the art to modify Hung et al.'s power supply clamp circuit by utilizing the technique taught by Carobolante for the purpose of confining a voltage at the second node in a desired voltage range.

With respect to claim 3, Hung et al. teaches an ESD protection circuit that utilizes an RC branch as the voltage generator of the power supply clamp circuit, which comprises a resistor 602 having one end of the resistor electrically connected to the voltage source and another end of the resistor electrically connected to the first node N1; and a capacitor 604 having one end of the capacitor electrically connected to the first node N1 and another end of the capacitor connected to ground as disclosed in Col. 6, lines 4-6 and lines 10-11. With respect to claim 5, Hung et al. teaches that the capacitor 604 of the voltage

generator comprises an NMOS transistor having a drain and a gate electrically connected to a substrate as explained in Col. 6, lines 7-10 and Fig. 6A.

With respect to claim 4, neither Hung et al. nor Carbolante explicitly disclose that the resistor of the first voltage generator comprises metal wiring. However, the use of both metal wire and carbon composition type resistors are known. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use any known conventional type of resistor in the voltage generator of Hung et al. as modified by Carbolante

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hung et al. in view of Carbolante as applied above and further in view of Usenko, Patent No. 6,690,561. With respect to claim 2, Hung et al. as modified by Carbolante is silent as to the formation process of the drain of the second NMOS transistor. Usenko teaches a fabrication method for semiconductor devices such as CMOS and NMOS in which the drain of the NMOS has P+ implantation dosage in an ion implantation process as disclosed in Col. 10, lines 39-40. It would have been obvious to one of ordinary skill in the art to use the ion implantation process of Usenko in the power supply circuit of Hung as modified by Carbolante as one of any known forms of fabrication for the device such as deposition, etching, ion implantation or thermal diffusion of dopants.

4. ***Allowable Subject Matter***

Claims 6-8, 10-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance: Hung et al. teaches a gate-coupled ESD protection circuit which utilizes a resistor and a capacitor as a voltage generator but does not have a second voltage source that is independent from the first voltage source, the second voltage comprising a resistor, a third PMOS transistor, and a third NMOS transistor as a voltage generator. This is not anticipated or rendered obvious by the prior art reference.


5. ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn Feild can be reached on 571-272-2092. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public

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PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


LYNN FEILD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800